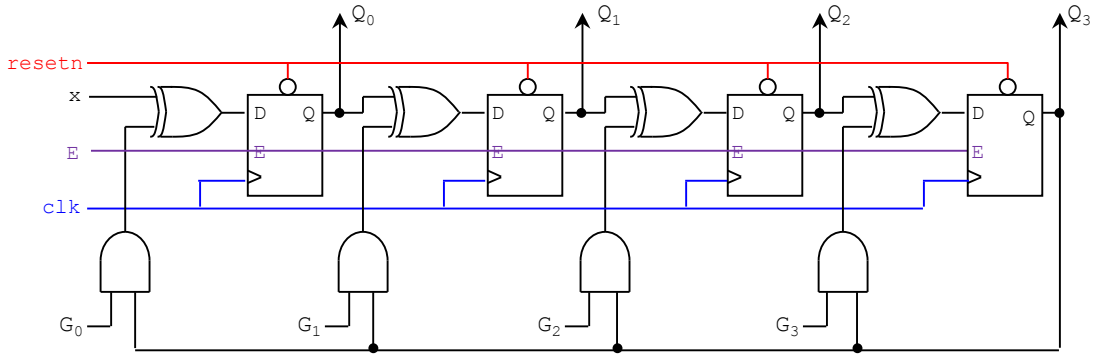
Final Exam

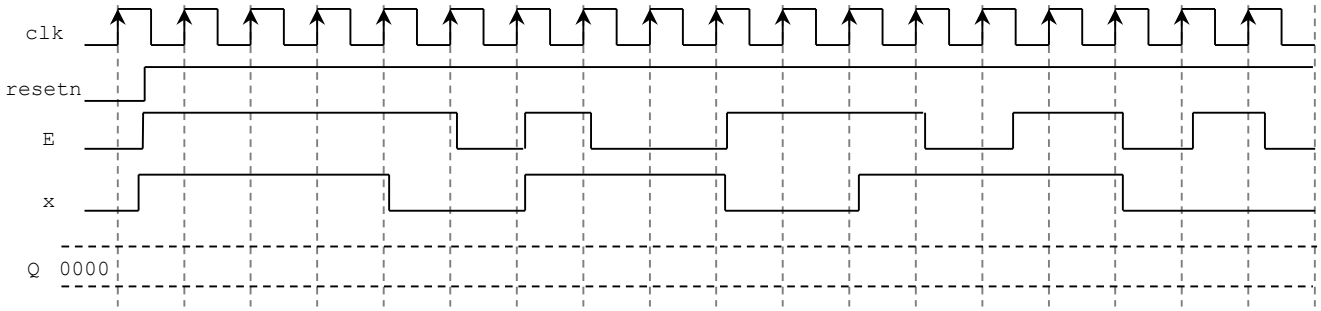
(December 14th @ 7:00 pm)

Presentation and clarity are very important! Show your procedure!

Problem 1 (12 pts)

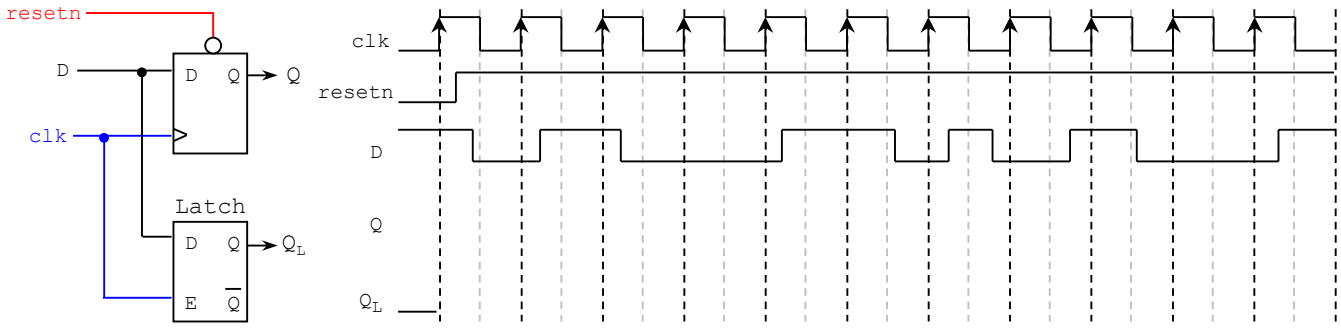
- Complete the timing diagram of the following circuit. $G = G_3G_2G_1G_0 = 0110$, $Q = Q_3Q_2Q_1Q_0$



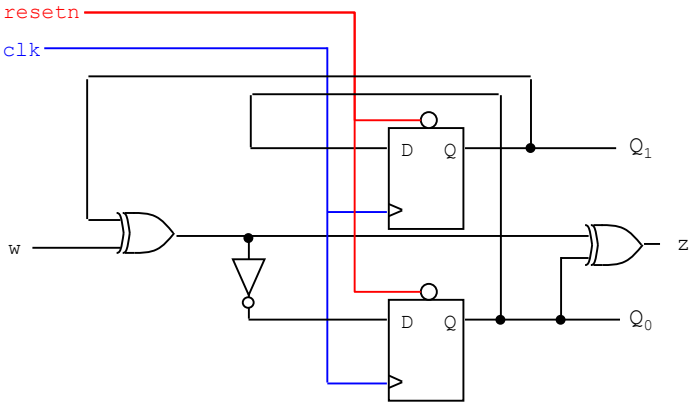


Problem 2 (19 pts)

- Complete the timing diagram of the circuit shown below: (8 pts)

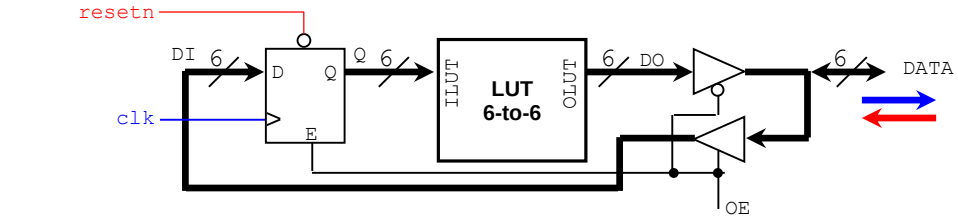


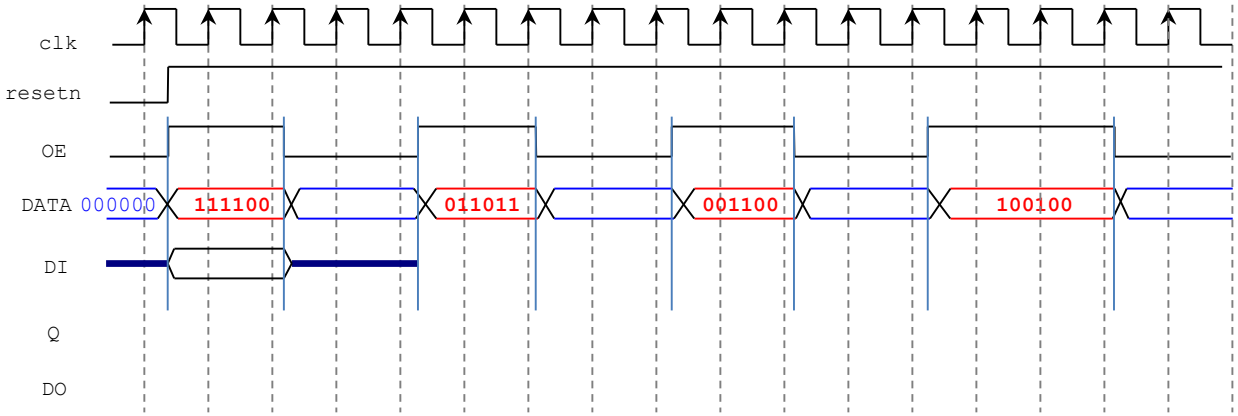
- Provide the State Diagram (any representation), the Excitation Table, and the Excitation equations of the following Finite State Machine: (11 pts)



PROBLEM 3 (10 PTS)

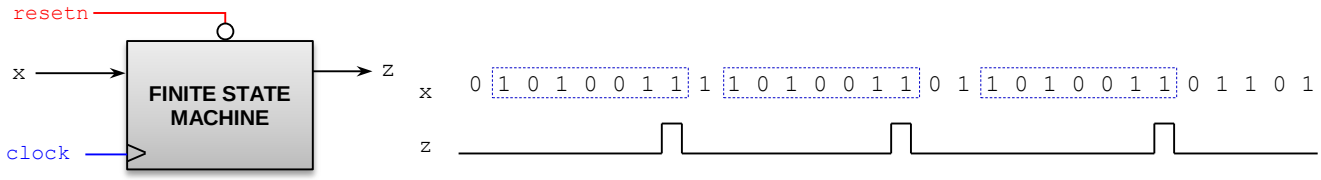
- Given the following circuit, complete the timing diagram.
  The LUT 6-to-6 implements the following function: $OLUT = \lceil sqrt(ILUT) \rceil$, where $ILUT$ is a 6-bit unsigned number.
  For example $ILUT = 35\ (100011_2) \rightarrow OLUT = \lceil sqrt(35) \rceil = 6\ (000110_2)$





PROBLEM 4 (23 PTS)

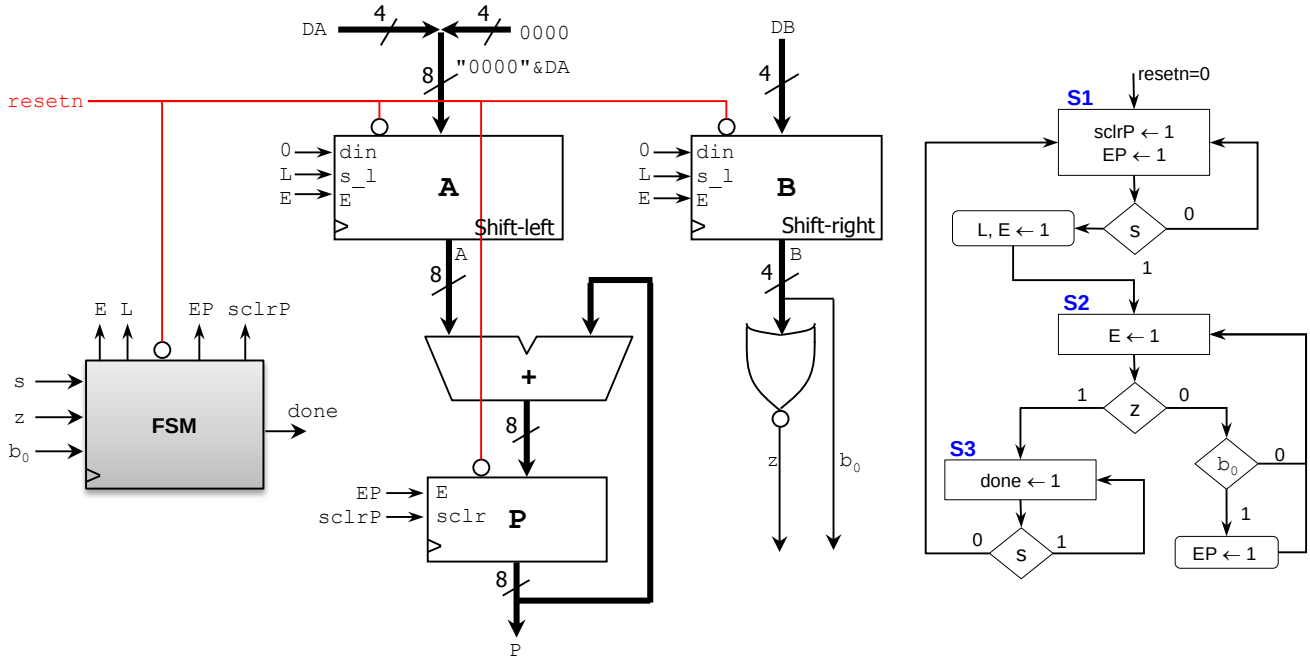
- Sequence detector: The machine has to generate $z = 1$ when it detects the sequence 1010011. Once the sequence is detected, the circuit looks for a new sequence.

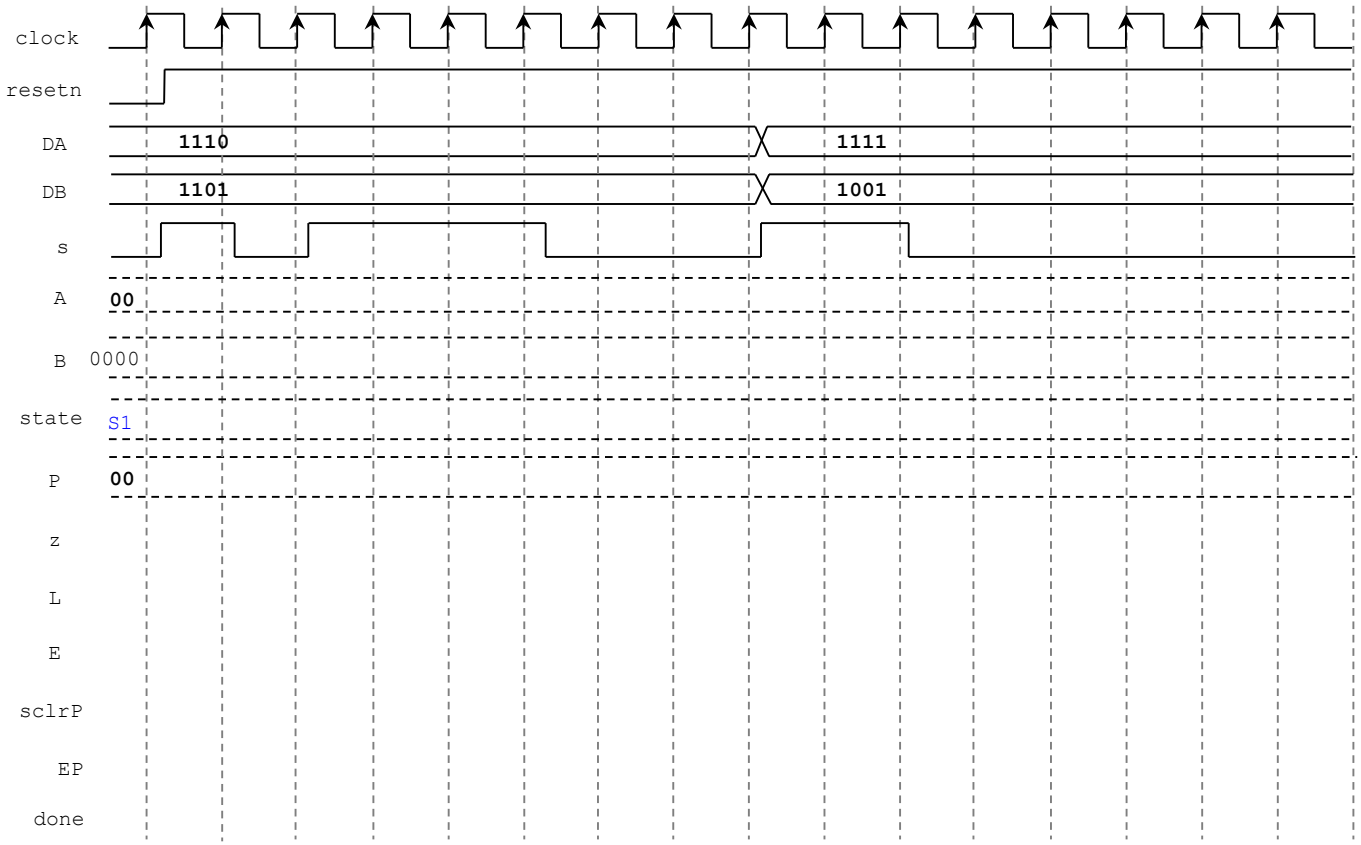


- Draw the State Diagram (any representation), State Table, and the Excitation Table of this circuit with input x and output z. Is this a Mealy or a Moore machine? Why? (15 pts)
- Provide the excitation equations (simplify your circuit using K-maps or the Quine-McCluskey algorithm) (5 pts)
- Sketch the circuit. (3 pts)

PROBLEM 5 (20 PTS)

- Complete the following timing diagram (A and P are specified as hexadecimals) of the following Iterative unsigned multiplier. The circuit includes an FSM (in ASM form) and a datapath circuit.
  Register (for P): $sclr$: synchronous clear. Here, if $sclr = E = 1$, the register contents are initialized to 0.
  Parallel access shift registers (for A and B): If $E = 1$: $s\_l = 1 \rightarrow$ Load, $s\_l = 0 \rightarrow$ Shift





PROBLEM 6 (16 PTS)

- Draw the State Diagram (in ASM form) of the FSM whose VHDL description in shown below. Is it a Mealy or a Moore FSM?
- Complete the Timing Diagram.

```
library ieee;
use ieee.std_logic_1164.all;

entity circ is
   port ( clk, resetn: in std_logic;
          r, p, q: in std_logic;
          x, w, z: out std_logic);
end circ;
```

```
architecture behavioral of circ is
   type state is (S1, S2, S3);
   signal y: state;
begin
  Transitions: process (resetn, clk, r, p, q)
  begin
     if resetn = '0' then y <= S1;
     elsif (clk'event and clk = '1') then
        case y is
          when S1 =>
            if r = '0' then
               y <= S2;
            else
               if p = '1' then y <= S3; else y <= S1; end if;
            end if;

          when S2 =>
            if q = '1' then y <= S1; else y <= S3; end if;

          when S3 =>
            if p = '1' then y <= S3; else y <= S2; end if;

        end case;
     end if;
  end process;

  Outputs: process (y, r, p, q)
  begin
      x <= '0'; w <= '0'; z <= '0';
      case y is
         when S1 => if r = '1' then
                       w <= '1';
                       if p = '0' then
                          x <= '1';
                       end if;
                    end if;

         when S2 => if p = '1' then x <= '1'; end if;
                    if q = '0' then z <= '1'; end if;

         when S3 => if p = '0' then x <= '1'; end if;
      end case;
  end process;
end behavioral;
```